REMARKS

Reconsideration of the above-identified application in view of the preceding amendments and following remarks is respectfully requested. Claims 1-9 are pending in this application. By this Amendment, Claims 1, 3 and 7 have been amended. Support for these amendments can be found in paragraphs 12-15 and Figure 2 among other places in the specification.

In the Office Action, Claims 1-9 were rejected under 35 U.S.C. § 103 (a) over the AAPA in view of U.S. Patent No. 5,648,281 to Williams et al. The Examiner's grounds for rejection are herewith traversed, and reconsideration is respectfully requested.

The AAPA merely discloses a N^+ type electrode layer 118 outside the active region of a power transistor.

Williams et al. disclose P+ sinkers 346 surrounding a PNP transistor 330 (see col. 24, line 23) and an N+ sinker 348 surrounding a P-well 344 (see col. 24, line 35). The N+ sinkers 348 are formed extending down from the surface of the wafer to the N buried layer 340 (see col. 24, lines 30-33). In other words, the N+ sinkers 348 are not under an N+ type electrode layer. Further, the active region of the PNP transistor in Williams et al. is inside of the P+ sinkers 346. Neither Figure 28 nor Figure 28A of Williams et al. disclose an electrode portion between the P+ sinkers 346 and which passes through a P buried layer 342 to an N buried layer 340. Thus, there is no teaching, motivation or suggestion in Williams et al. to provide an electrode portion of the N+ buried layer 340 in the power transistor active region as is relevant to Claim 9 discussed below.

There is nothing in either of these references that discloses or suggests, either alone or

in combination, in whole or in part, the device defined by Claims 1 and 9 of the subject application.

In particular for amended Claim 1, neither the AAPA nor Williams et al. disclose or suggest, either alone or in combination, in whole or in part, a power transistor including a plurality of vertical PNP transistors formed on a P-type silicon substrate, an N^+ type buried layer formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors from each other, and at least one electrode portion of the N^+ type buried layer, which has an N^+ type diffusion layer contacting the N^+ type buried layer, wherein the at least one electrode portion is located in an active region of the power transistor surrounded from all around by the vertical PNP transistors. As a result and as noted in the specification (see paragraph 12-15 among other places), the distance from each part of the N+ type buried layer to the electrode portion becomes shorter, and so the resistance thereof becomes smaller. Thus, the resistance distribution of pathways concerning parts of the buried layer can be uniformized, making it possible to suppress the occurrence of local leak currents. Also, malfunctions of the parasitic PNP transistors can be stabilized. Further, the limited design space of the power transistor can be used effectively without increasing the power transistor size, thus it is unnecessary to make complex pattern design.

In contrast, in Figure 28A, Williams et al. teach N+ sinkers 348 that surround the vertical PNP transistor 330 and correspond to electrode portions. As recited in Claim 1, the vertical PNP transistor surrounds the electrode portion of the N+ type buried layer from all around to prevent the need to make the power transistor size unnecessarily large. Accordingly, Claim 1 has a structure that is not shown or suggested in the prior art. Thus, Claim 1 and each of the claims depending therefrom are not rendered obvious by

the combination of references cited by the Examiner and withdrawal of the rejection under 35 U.S.C. §103 (a) is respectfully requested.

Turning to Claim 9, neither the AAPA nor Williams et al. disclose or suggest, either alone or in combination, in whole or in part, a power transistor having suppression of problematic leak current, the power transistor including a plurality of vertical PNP transistors formed on a P-type substrate, each PNP transistor having a P^+ type collector, an N+ type base well formed at a base region, a P^+ type emitter layer and an N^+ type base layer, P^+ type collector buried layers formed under the N^+ type base well, an N^+ type buried layer isolating the P-type substrate from the P^+ type collector, an N-type epitaxial layer formed over a surface of the P-type substrate, an N^+ type electrode layer and a plurality of N^+ type diffusion layers formed at electrode portions within an active region under, contacting and surrounding the N^+ type electrode layer to reduce resistance of the N-type epitaxial layer by extending therethrough to contact the N^+ type buried layer, wherein at least one of the N^+ type diffusion layers passes between the P^+ type collector buried layers. Neither of the cited references disclose the N+ type diffusion layers being under N+ type electrode layers as noted above. Moreover, neither the AAPA nor Williams et al. disclose electrode portions of a N+ buried layer in an active region of a power transistor. Thus, there is nothing in either of these references that discloses or suggests, either alone or in combination, in whole or in part, the device defined by Claim 9 of the subject application. Thus, for at least these reasons, Claim 9 is not obvious in view of the cited combination and allowance is respectfully requested.

It is respectfully submitted that all of the claims now remaining in this application, namely Claims 1-9, are in condition for allowance, and such action is earnestly

solicited. Any additional fees or overpayments due as a result of filing the present paper may be applied to Deposit Account No. 04-1105.

If after reviewing this amendment, the Examiner believes that a telephone interview would facilitate the resolution of any remaining matters the undersigned attorney may be contacted at the number set forth herein below.

Respectfully submitted,

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George Chaclas

George N. Chaclas, Reg. No. 46,608
Edwards, Angell, Palmer & Dodge LLP
Attorney for Applicant
P.O. Box 55874
Boston, MA 02205
Tel: (401) 276-6653
Fax: (888) 325-1684
Email: gchaclas@eapdlaw.com